# CT-PCDM

## Pulse Code Demodulation Trainer


*Salient Features:*
It has facility to generate the binary code of input signal, using analog to digital converter and time division multiplexing of two such PCM data stream.

*Specifications:*
It has facility to demultiplexed the binary data stream and recover of the original waveform, using digital to analog conversion
Input channels: 2 numbers time division multiplexed code (de-modulated)
Receiver clock: Generated by phase lock loop (Fast mode)
Parity check facility: Even, odd, hamming, No-parity
Error Detection: Single bit error detection on LED, when even or odd parity mode is selected
Correction facility: Single bit error detection & correction, when hamming parity code is selected
Low pass filter cut-off points: 3.4KHz
LED Display: At every functional block for examination of Digital data and control signal
Power Supply: In-Built

*List of Experiments:*
Study of 2 channel time division demultiplexing and pulse code demodulation
Study of error check code logic using odd parity, even parity and hamming parity
Study of effect of single bit error detection i odd parity and even parity mode ad single bit error correction i hamming parity mode
To learn the function of phase lock loop (PLL) to a receiver clock generator and frequency synthesizer

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